IN THE CLAIMS

Please amend the claims as follows:

1. (original) A semiconductor device (10) with a substrate and a semiconductor body (1) of silicon which comprises a field effect transistor having a source region (2) which borders on the surface of the semiconductor body (1) and which is connected to a lower-doped, thinner source region extension (2A) and having a drain region (3) which borders on the surface of the semiconductor body (1) and which is connected to a lower-doped, thinner drain region extension (3A), which regions (2, 3) and extensions (2A, 3A) are of a first conductivity type, and having a channel region (4) situated between said regions and extensions, which channel region is of a second conductivity type, opposite to the first conductivity type, and having a gate electrode (6) separated from the channel region (4) by a dielectric region (5), the source region (2) and the drain region (3) being provided with a connection region (2B, 3B) containing a metal silicide, characterized in that the source region (2) and the source region extension (2A), and the drain region (3) and the drain region extension (3A) are in each case connected with each other via an intermediate region (2C, 3C) of the first conductivity type the thickness and doping concentration of which range between those of the region (2, 3) and the extension

(2A, 3A) which are connected with one another by the intermediate region (2C, 3C).

2. (original) A semiconductor device (10) as claimed in claim 1, characterized in that the connection region (2B, 3B) is recessed in the semiconductor body (1).

3. (currently amended) A semiconductor device (10) as claimed in claim 1~~ or 2~~, characterized in that a spacer (7) of an electrically insulating material is situated on the semiconductor body (1) on either side of the gate electrode (6), and the intermediate region (2C, 3C) and the associated extension (2A, 3A) are situated below these spacers (7), viewed in projection.

4. (currently amended) A semiconductor device as claimed in claim 1~~, 2 or 3~~, characterized in that the intermediate region (2C, 3C) is formed by means of ion implantation.

5. (original) A method of manufacturing a semiconductor device (10) with a substrate and a semiconductor body (1) of silicon which comprises a field effect transistor, wherein, at the surface of the semiconductor body (1), a source region (2) is formed which is connected with a lower-doped, thinner source region extension (2A)

and a drain region (3) is formed which is connected with a lower-doped, thinner drain region extension (3A), which regions (2, 3) and extensions (2A, 3A) are provided with a first conductivity type, and between which a channel region (4) of a second conductivity type, opposite to the first conductivity type, is formed which is provided with a dielectric region (5) on which a gate electrode (6) is formed, and wherein the source region (2) and the drain region (3) are provided with a connection region (2B, 3B) which comprises a metal silicide, characterized in that an intermediate region (2C, 3C) of the first conductivity type is formed in each case between the source region (2) and the source region extension (2A) and between the drain region (3) and the drain region extension (3A), which intermediate region is provided with a thickness and a doping concentration which range between those of the region (2, 3) and the extension (2C, 3C) which are connected to one another by the intermediate region (2C, 3C).

6. (original) A method as claimed in claim 5, characterized in that the metal silicide is formed by providing a metal (8) on the semiconductor body (1) and allowing this metal to react with silicon of the semiconductor body (1) to form the metal silicide of the connection region (2B, 3B).

7. (currently amended) A method as claimed in claim 5~~ or 6~~, characterized in that a spacer (7) of an electrically insulating material is formed on either side of the gate electrode (6), and the intermediate region (2C, 3C) is formed by an ion implantation (I_2) of a doping element of the first conductivity type, the ion implantation (I_2) being carried out at an acute angle (A) with the normal to the surface of the semiconductor body (1).

8. (original) A method as claimed in claim 7, characterized in that for the angle (40) at which the ion implantation (I_2) is carried out an angle (A) between 0 degrees and 45 degrees is chosen, and preferably an angle (A) between 20 and 40 degrees.

9. (currently amended) A method as claimed in claim 7~~ or 8~~, characterized in that the ion implantation (I_2) is carried out at an energy between 0.5 and 10 keV, and a flux between 5×10^{13} at/cm^2 and 5×10^{14} at/cm^2.

10. (currently amended) A method as claimed in claim 7~~, 8 or 9~~, characterized in that the source region (2) and the drain region (3) are also formed by means of an ion implantation (I_1), and the intermediate region (2C, 3C) is formed immediately before or after the formation of the source region (2) and the drain region (3),

and all these regions (2, 2C, 3, 3C) are tempered in the same heat treatment.